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INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

07 DEC 2004

Applicant's or agent's file reference P56966PC00	**FOR FURTHER ACTION**	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
International application No. PCT/NL 02/00436	International filing date *(day/month/year)* 03.07.2002	Priority date *(day/month/year)*
International Patent Classification (IPC) or both national classification and IPC H03L7/093		
Applicant TELEFONAKTIEBOLAGET L.M. ERICSSON ET AL.		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 6 sheets, including this cover sheet.

   ☒ This report is also accompanied by ANNEXES, i.e. sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 4 sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the opinion
   - II ☐ Priority
   - III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - IV ☐ Lack of unity of invention
   - V ☒ Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
   - VI ☐ Certain documents cited
   - VII ☐ Certain defects in the international application
   - VIII ☐ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
13.01.2004	11.11.2004
Name and mailing address of the international preliminary examining authority: European Patent Office - P.B. 5818 Patentlaan 2 NL-2280 HV Rijswijk - Pays Bas Tel. +31 70 340 - 2040 Tx: 31 651 epo nl Fax: +31 70 340 - 3016	Authorized Officer Balbinot, H Telephone No. +31 70 340-3344

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No. PCT/NL 02/00436

I. Basis of the report

1. With regard to the **elements** of the international application *(Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17))*:

Description, Pages

1-11 as originally filed

Claims, Numbers

1-16 received on 01.10.2004 with letter of 30.09.2004

Drawings, Sheets

1/6-6/6 as originally filed

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.

   These elements were available or furnished to this Authority in the following language: , which is:

   ☐ the language of a translation furnished for the purposes of the international search (under Rule 23.1(b)).

   ☐ the language of publication of the international application (under Rule 48.3(b)).

   ☐ the language of a translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

   ☐ contained in the international application in written form.

   ☐ filed together with the international application in computer readable form.

   ☐ furnished subsequently to this Authority in written form.

   ☐ furnished subsequently to this Authority in computer readable form.

   ☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

   ☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. The amendments have resulted in the cancellation of:

   ☐ the description, pages:

   ☐ the claims, Nos.:

   ☐ the drawings, sheets:

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)).

   (Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.)

6. Additional observations, if necessary:

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	1-16
	No:	Claims	NONE
Inventive step (IS)	Yes:	Claims	1-16
	No:	Claims	NONE
Industrial applicability (IA)	Yes:	Claims	1-16
	No:	Claims	NONE

2. Citations and explanations

   see separate sheet

Re Item V

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Reference is made to the following documents:
   D1: WO 95/31861 A (COPELAND MILES ALEXANDER ;RILEY THOMAS ATKIN DENNING (CA)) 23 November 1995 (1995-11-23)
   D2: BEARDS R D ET AL: "AN OVERSAMPLING DELTA-SIGMA FREQUENCY DISCRIMINATOR" IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: ANALOG AND DIGITAL SIGNAL PROCESSING, IEEE INC. NEW YORK, US, vol. 41, no. 1, 1994, pages 26-32, XP000439300 ISSN: 1057-7130
   D3: J. B. Encinas "PHASE LOCKED LOOPS", Chapman & Hall, London, GB 1993, ISBN 0 412 48260 6, pages 11-29

2. The document D1 is regarded as being the closest prior art to the subject-matter of claim 1 and shows (the references in parentheses applying to this document):
   a locked loop circuit (see fig. 1) at least including:
   - a loop input (Fd);
   - a detector section (103-105) for detecting a difference between an input signal (Fd) and a reference signal (Do), said detector section (103-105) having a detector input connected to said loop input (Fd), a reference input (Do) and a detector output (the output signal of D/A converter 105) for outputting a signal related to said difference (see page 1, line 32 to page 2, line 1);
   - a controlled oscillator (107) having an input communicatively connected to said detector output and an oscillator output connected to a loop output; and
   - a feedback circuit (101, 102, 108) connecting said oscillator output to said reference input (Do), wherein said feedback circuit includes a device (frequency discriminator 101; see details thereof in fig. 2 and 3a) having a transfer function with at least one zero (see the present application page 10, lines 22-24 and comment 1 below), and the look loop circuit has a closed loop transfer function without zeros (see comment 2 below).

   Comment 1: it is noted that another embodiment of a suitable frequency discriminator for use in D1 is said to be disclosed in D2 (see D1, see page 6, lines 23-30), so that the relevant teachings of D2 may be considered as being included into D1. According to the present application itself (see page 11, lines 11-15), the frequency discriminator disclosed in D2 has a transfer function which includes

a zero.

Comment 2: Although the single embodiment of the frequency locked loop circuit disclosed in details in D1 with reference to figure 1 does show a locked loop circuit having a closed loop transfer function with a zero, the teachings of D1 are not limited to such locked loop circuits: D1 explicitly recites in the section entitled "DISCLOSURE OF THE INVENTION" on page 1 that "Filters means **may** be provided between the differencing means and the digital-to-analog conversion means" (see page 1, lines 32-33) and "Where **both** the first-mentioned filter means and the second-mentioned filter means are included, a stabilizing zero means will **generally** be included to ensure stability of the frequency synthesizer circuit" (see page 2, lines 2-4) (emphasis added). It is therefore clear that the teachings of D1 are not limited to PLL's having a zero in the closed loop transfer function. In particular if the second integrating filter 106 (see fig. 1 of D1) were not used, then the stabilizing zero in the first filter 104 would not need to be provided, as is clear from the above-mentioned passage of D1 and from D3, which is a reference book in the field of phase locked loops, see paragraph 2.4.1 thereof, which clearly explains that a PLL having a lowpass filter with no zeros and a single pole is unconditionally stable (see D3, page 19, line 3). As stated in D3, page 21, lines 1-4, such PLL's have advantages and disadvantages since they are simpler but do not allow simultaneous optimization of bandwidth, damping factor and gain. Such PLLs having no zero in the closed loop are yet used in a number of applications. The same reasoning also applies if the first filter 104 were not used and only the second filter 106 were used.

2.1 The subject-matter of claim 1 thus differs from this known locked loop circuit in that it is a **phase**-locked loop circuit and in that said detector section is a **phase** detector section for detecting a **phase** difference between said input signal and said reference signal and for outputting a signal related to said **phase** difference.

Therefore the subject-matter of claim 1 is new.

2.2 The problem to be solved by the present invention may be regarded as the provision

of a phase locked loop wherein initial phase differences can be compensated for so as to generate a more stable output signal.

2.3 Starting from D1, extensive modifications of the synthesizer disclosed therein would be required to adapt the synthesizer of D1 such that an initial phase difference is reduced and phase locked. In particular, the inputs of the detector section 103-105 would have to be modified to contain information about the initial phase, which would in turn would require a complete change of the structure of the feedback loop of D1, since the decimator 102, the frequency discriminator 101 as well as the input signal Fd would all have to be suitably adapted.

Furthermore such modifications are neither disclosed nor suggested by the available prior art and are considered to be beyond the scope of current practice of the person skilled in the art.

Therefore it is considered that the skilled person would not amend the teachings of D1 so as to arrive at a phase locked loop according to claim 1. Hence claim 1 is considered to involve an inventive step.

3 Claim 14 is directed to a method for generating a periodic signal corresponding to the phase locked loop circuit according to claim 1. Hence its subject-matter is new over D1, which is also considered to represent the closest prior art to that claim, for similar reasons to those given above for claim 1.

4. Claims 2-13, 15 and 16 are dependent on claim 1 and as such also meet the requirements of the PCT with respect to novelty and inventive step.

5. Contrary to the requirements of Rule 5.1(a)(ii) PCT, the relevant background art disclosed in the document D1 is not mentioned in the description, nor is this document identified therein.

- 1. 10. 2004

(55)

CLAIMS

1. A phase locked loop(PLL) circuit (1) at least including:
a loop input (11);
a phase detector section (2,3) for detecting a phase difference between an input signal and a reference signal, said phase detector section (2,3) having a detector input connected to said loop input, a reference input and a detector output for outputting a signal related to said phase difference;
a controlled oscillator (4) having an input communicatively connected to said detector output and an oscillator output connected to
a loop output (12); and
a feedback circuit (13) connecting said oscillator output to said reference input,
wherein
said feedback circuit includes a device (7;71-74) having a transfer function with at least one zero, and the phase locked loop circuit (1) has a closed loop transfer function without zeros.

2. A phase locked loop circuit as claimed in claim 1, further including a filter section (4) having a filter input connected to said detector output and a filter output connected to said oscillator input.

3. A phase locked loop circuit as claimed in claims 1 or 2 , wherein said feedback circuit further includes at least one frequency divider device (6;7;72;73).

4. A phase locked loop circuit as claimed in claim 3, wherein said frequency divider device is connected to a delta-sigma modulator device (8).

5. A phase locked loop circuit as claimed in claim 3 or 4, wherein said frequency divider device (6;7;72;) has a transfer function with said zero.

6. A phase locked loop circuit as claimed in any one of claims 3-5, wherein said feedback circuit includes a first frequency divider device (6) and a second frequency divider device (7;72;73), said second frequency divider device having a transfer function with a zero.

7. A phase locked loop circuit as claimed in claim 6, wherein said first frequency divider device (6) and said second frequency divider device (7;72;73) are connected in parallel and wherein an output of the first frequency divider device and an output of the second frequency divider device are each connected to an input of a second combiner device (200), and wherein an output of the second combiner device is connected to the reference input of the phase detector section (2,3).

8. A phase locked loop circuit as claimed in claim 6, wherein an output of the second frequency divider device (73) is connected to an first input of a second combiner device (210), a second input of the second combiner device is connected to the output of the phase detector, an output of the second combiner device is communicatively connected to the VCO, and wherein:
the second divider device comprises a phase detector section and has a transfer function with said zero.

9. A phase locked loop circuit as claimed in any one of claims 3-5, wherein said frequency divider device (6) is connected in series with a device (71;74;75) having a transfer function with a zero.

10. A phase locked loop circuit as claimed in claim 9 wherein said device (71;75) having a transfer function with a zero has an input connected to the controlled oscillator (5) and an output connected to an input (61) of the frequency divider (6)

11. A phase locked loop circuit as claimed in claim 9, wherein said device (71;75) having a transfer function with a zero has an input connected to an output of the frequency divider (6) and an output connected to an input of the phase detector section.

12. A phase locked loop circuit as claimed in claims 4 and 11, wherein said device (74) having a transfer function with a zero has a first input (741) connected to said delta-sigma modulator (8) and a second input (742) connected to the output of the frequency divider (6).

13. A phase locked loop circuit as claimed in claim 10, wherein said device (71;75) having a transfer function with a zero comprises:
a device (75) with a transfer function equal to $\tau_s s$, said device with a transfer function equal to $\tau_s s$ with a device input (751) connected to the output of the oscillator (4),
said device (71;75) having a transfer function with a zero further comprising:
a combiner device (22) with:
a first combiner input connected to the output of the device (75) with a transfer function equal to $\tau_s s$;
a second combiner input connected to the input of the device (75) with a transfer function equal to $\tau_s s$, and
a combiner output (752) connected to the input of the frequency divider device (6).

14. A method for generating a periodic signal, at least comprising:
receiving a periodic signal of a first frequency;
comparing a phase of said periodic signal with a phase of a reference signal
generating a difference signal relating to a phase difference between said periodic signal and said reference signal;

filtering said difference signal;
generating an output signal with a frequency corresponding to an amplitude of said difference signal;
transmitting said output signal further;
generating said reference signal by changing said output signal such that the frequency of the output signal is lowered;
wherein for said changing of said output signal a feedback circuit having a transfer function with at least one zero, is used ,and said receiving a periodic signal until said transmitting said output signal involves a closed loop transfer function without zeros.

15. An electronic device including a phase locked loop circuit as is claimed in any one of claims 1-13.

16. A wireless communication device, at least comprising:
a phase locked loop circuit as is claimed in any one of claims 1-13.